

## EAST SEARCH

7/26/05

L#	Hits	Search String	Databases
S1	34984	((integrated or digital) near2 circuit\$1) with (simulat\$3 or test\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	21	S1 and ("test bench" with stimulus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	478	S1 and ((DUT or "device under test" or device) near2 model)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S4	13	S1 and (((DUT or "device under test" or device) near2 model) with "test bench")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S5	35	S3 and (model with stimulus)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	76	S1 and ("test bench" with model)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	52	S3 and (captur\$3 with (output or simulation))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	254	S1 and ("test bench" with stimulus) or (((DUT or "device under test" or device) near2 model)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	254	S1 and ("test bench" with stimulus) or (((DUT or "device under test" or device) near2 model)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	1	S3 and ("test bench" with communicat\$3 with (DUT or "device under test" or device))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	257	S3 and (direction\$5 or "pin data" or mask\$3 or cyclize\$1 or comment\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S22	103	S3 and (mask\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S24	3	S3 and (cyclize\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S25	4	S3 and (mask\$3 and comment\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	1	S3 and (retargettable with (post near2 process\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	20	S3 and (post near2 process\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	1	S3 and (formatted with (pattern near2 file\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S30	5	S3 and (formatted with pattern)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S31	75	S3 and ((fault near2 simulat\$3) or (Virtual near2 (simulat\$3 or tester)) or "automatic test equipr	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S32	9	S3 and ("data pattern" with generat\$3) or (reusable with "test bench"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	148	S2 or S6 or S5 or S7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	15	S7 and ("strobe timing" or opcode or "mixed signal" or "memory content")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	74	S3 and ("strobe timing" or opcode or "mixed signal" or "memory content")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	13	S3 and (automatic\$3 with generat\$3 with (test near2 pattern\$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	1	S3 and ("test bench" with generat\$3 with (model or stimulus))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S16	11	S3 and ("test bench" with communicat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S45	34464	((integrated or digital) near2 circuit\$1) with (tester or test\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S46	66	S45 and ((tester or test\$3) with opcode\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S47	202	S45 and ("test bench")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S48	15	S46 and ("strobe timing" or "mixed signal" or "memory content")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S49	885	S45 and ("strobe timing" or "mixed signal" or "memory content")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S50	42	S47 and S49	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S51	3	S47 and S46	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S52	106	S51 or S48 or S50 or S46	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S53	34464	((integrated or digital) near2 circuit\$1) with (tester or test\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S54	66	S53 and ((tester or test\$3) with opcode\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S55  
S56  
S57  
S59  
S60  
S58  
S61  
S62

202 S53 and ("test bench")  
15 S54 and ("strobe timing" or "mixed signal" or "memory content")  
3 S55 and S54  
885 S53 and ("strobe timing" or "mixed signal" or "memory content")  
42 S55 and S59  
66 S57 or S56 or S54  
106 S57 or S56 or S60 or S54  
4 S53 and ((tester or "testing equipment") with opcode\$1)

US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM\_TDB  
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## Results of search set S51:

Document Kind	Codes Title	Issue Date	Current OR	Abstract
US 20050021275 A1	Method and system for test data capture and compression for electronic device analysis	20050127	702/122	
US 20040187000 A1	Apparatus for authenticating memory space of an authorized accessory	20040923	713/171	
US 20040078674 A1	Methods and apparatus for generating functional test programs by traversing a finite state mod	20040422	714/33	
US 20030212935 A1	Circuit and method for accelerating the test time of a serial access memory device	20031113	714/719	
US 20030149949 A1	Verification of embedded test structures in circuit designs	20030807	716/4	
US 20030079166 A1	Electronic device	20030424	714/727	
US 20020163351 A1	Method for producing test patterns for testing an integrated circuit	20021107	324/765	
US 20020077782 A1	Secured microcontroller architecture	20020620	702/185	
US 6836868 B1	High-speed algorithmic pattern generator	20041228	714/743	
US 6834338 B1	Microprocessor with branch-decrement instruction that provides a target and conditionally mod	20041221	712/234	
US 6757819 B1	Microprocessor with instructions for shifting data responsive to a signed count value	20040629	712/300	
US 6748521 B1	Microprocessor with instruction for saturating and packing data	20040608	712/221	
US 6745319 B1	Microprocessor with instructions for shuffling and dealing data	20040601	712/223	
US 6675339 B1	Single platform electronic tester	20040106	714/744	
US 6671797 B1	Microprocessor with expand instruction for forming a mask from one bit	20031230	712/224	
US 6449741 B1	Single platform electronic tester	20020910	714/724	
US 6321352 B1	Integrated circuit tester having a disk drive per channel	20011120	714/724	
US 6249893 B1	Method and structure for testing embedded cores based system-on-a-chip	20010619	714/741	
US 6237123 B1	Built-in self-test controlled by a token network and method	20010522	714/733	
US 6205407 B1	System and method for generating test program code simultaneously with data produced by A	20010320	702/119	
US 6189253 B1	Analog clock module	20010213	327/105	
US 6181151 B1	Integrated circuit tester with disk-based data streaming	20010130	324/765	
US 6163874 A	Apparatus and method for doubling speed of random events generator	20001219	716/4	
US 6154865 A	Instruction processing pattern generator controlling an integrated circuit tester	20001128	714/743	
US 6112298 A	Method for managing an instruction execution pipeline during debugging of a data processing s	20000829	712/227	
US 6101622 A	Asynchronous integrated circuit tester	20000808	714/724	

US 6092225 A	Algorithmic pattern generator for integrated circuit tester	20000718 714/724
US 6081885 A	Method and apparatus for halting a processor and providing state visibility on a pipeline phase	20000627 712/227
US 6065106 A	Resuming normal execution by restoring without refetching instructions in multi-word instruction	20000516 712/24
US 6055649 A	Processor test port with scan chains and data streaming	20000425 714/30
US 6016555 A	Non-intrusive software breakpoints in a processor instruction execution pipeline	20000118 714/35
US 5978947 A	Built-in self-test in a plurality of stages controlled by a token passing network and method	19991102 714/733
US 5970241 A	Maintaining synchronism between a processor pipeline and subsystem pipelines during debug	19991019 712/227
US 5925145 A	Integrated circuit tester with cached vector memories	19990720 714/738
US 5894484 A	Integrated circuit tester with distributed instruction processing	19990413 714/738
US 5838694 A	Dual source data distribution system for integrated circuit tester	19981117 714/738
US 5831991 A	Methods and apparatus for electrically verifying a functional unit contained within an integrated	19981103 714/724
US 5828825 A	Method and apparatus for pseudo-direct access to embedded memories of a micro-controller	19981027 714/27
US 5805792 A	Emulation devices, systems, and methods	19980908 714/28
US 5805610 A	Virtual channel data distribution system for integrated circuit tester	19980818 712/211
US 5796974 A	Microcode patching apparatus and method	19980630 700/86
US 5774358 A	Method and apparatus for generating instruction/data streams employed to verify hardware im	19980512 714/718
US 5751729 A	Method and apparatus for efficient self testing of on-chip memory	19980217 714/733
US 5719880 A	On-chip operation for memories	19971014 714/720
US 5677913 A	Method and apparatus for efficient self testing of on-chip memory	19970805 340/870.01
US 5654698 A	Missile telemetry data interface circuit	19970617 714/42
US 5640509 A	Programmable built-in self-test function for an integrated circuit	19970422 714/727
US 5623503 A	Method and apparatus for partial-scan testing of a device using its boundary-scan port	19970311 702/117
US 5610826 A	Analog signal monitor circuit and method	19970311 340/870.07
US 5610598 A	Missile telemetry data interface circuit	19970121 710/5
US 5596734 A	Method and apparatus for programming embedded memories of a variety of integrated circuits	19961119 702/119
US 5576980 A	Serializer circuit for loading and shifting out digitized analog signals	19950627 714/733
US 5428770 A	Single-chip microcontroller with efficient peripheral testability	19950307 324/158.1
US 5396170 A	Single chip IC tester architecture	19930413 714/739
US 5202889 A	Dynamic process for the generation of biased pseudo-random test patterns for the functional v	19921006 324/73.1
US 5153509 A	System for testing internal nodes in receive and transmit FIFO's	19910430 324/73.1
US 5012180 A	System for testing internal nodes	19900612 713/502
US 4933897 A	Method for designing a control sequencer	19890110 714/30
US 4797808 A	Microcomputer with self-test of macrocode	19880628 712/234
US 4754393 A	Single-chip programmable controller	19860909 370/241
US 4611320 A	Programmable testing analyzer	19841225 712/227
US 4490783 A	Microcomputer with self-test of microcode	19820713 714/734
US 4339819 A	Programmable sequence generator for in-circuit digital testing	19720307 324/115
US 3648175 A	COMPUTER-ORIENTATED TEST SYSTEM HAVING DIGITAL MEASURING MEANS WITH A	20021107
US 20020163351 A	Simulation output capturing method for testing integrated circuit manufacture, involves generati	19990410
RD 420018 A	Bootstrap mode testing and debugging of integrated circuits - configuring onchip microcontrolle	